WHAT IS CLAIMED IS:

1. A memory storing computer readable instructions permitting a MPEG-2 decoder to perform a DCT-domain linear contrast enhancement stretching function on each DCT coefficient block corresponding to luminance data prior to performing an inverse discrete cosine transform (IDCT) function.

2. The memory as recited in claim 1, wherein the MPEG-2 decoder implements the DCT-domain linear contrast enhancement stretching function by:

processing the DCT blocks of the intrablock type according to the expression

DCT[*output*] = {DCT[*input*] - DCT[β]} x α; and

processing the DCT blocks of the interblock type according to the expression

DCT[*output*] = DCT[*input*] x α,

where:

DCT[*output*] is the DCT transform of the output 8x8 block;

DCT[*input*] is the DCT transform of the input 8x8 block;

DCT[β] is the DCT transform of the 8x8 block whose every entry value is equal to β;

β is a shifting parameter, and

α is a stretching factor.

3. The memory as recited in claim 2, wherein the term DCT[β] has only one non-zero value.

4. The memory as recited in claim 2, wherein the DC coefficient of DCT[β] is equal to 8 x β.

5. The memory as recited in claim 1, wherein the memory comprises non-volatile random access memory electrically coupled to a microprocessor associated with the MPEG-2 decoder.

6. A method for implementing embedded DCT-domain linear contrast enhancement processing of a MPEG-2 video signal stream, comprising:

sorting DCT blocks contained in the MPEG-2 video signal stream into intrablocks, interblocks, and non-luminance blocks;

processing the intrablocks according to a first expression to thereby produce linear contrast enhanced intrablocks;

processing the interblocks according to a second expression to thereby produce linear contrast enhanced interblocks; and

inverse discrete cosine transforming the linear contrast enhanced intrablocks, the linear contrast enhanced interblocks, and the non-luminance blocks in the order corresponding to the order in which the corresponding intrablocks, interblocks, and non-luminance blocks occurred in the MPEG-2 video signal stream.

7. The method as recited in claim 6, wherein the first expression comprises:

$DCT[\mathit{output}] = \{DCT[\mathit{input}] - DCT[\beta]\} \times \alpha$;

where:

DCT[*output*] is the DCT transform of the output 8x8 block;

DCT[*input*] is the DCT transform of the input 8x8 block;

DCT[β] is the DCT transform of the 8x8 block whose every entry value is equal to β;

β is a shifting parameter, and

α is a stretching factor.

8. The method as recited in claim 6, wherein the second compression comprises:

$DCT[\mathit{output}] = DCT[\mathit{input}] \times \alpha$,

where:

DCT[*output*] is the DCT transform of the output 8x8 block;

DCT[*input*] is the DCT transform of the input 8x8 block; and

α is a stretching factor.

9. A MPEG-2 decoder receiving an MPEG-2 video stream containing discrete cosine transform (DCT) blocks which generates linear contrast enhanced DCT blocks applied to an inverse DCT processor.

10. The MPEG-2 decoder as recited in claim 9, further comprising:

a linear contrast enhancement processor receiving the DCT blocks and generating the linear contrast enhanced DCT blocks; and

the inverse DCT processor operatively coupled to the linear contrast enhancement processor.

11. The MPEG-2 decoder as recited in claim 10, further comprising:

a microprocessor which controls the linear contrast enhancement processor and the inverse DCT processor.

12. The MPEG-2 decoder as recited in claim 11, wherein the linear contrast enhancement processor is controlled based on instructions generated by the microprocessor in response to instructions stored in a memory coupled to the microprocessor.

13. The MPEG-2 decoder as recited in claim 11, wherein the linear contrast enhancement processor is controlled based on timing signals generated by the microprocessor.